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Attorney Docket No. 42390.P9429

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: )  
Jin Yang )  
Application No. 09/608,637 )  
Filed: June 30, 2000 )  
For: **METHODS FOR FORMAL** )  
**VERIFICATION ON A** )  
**SYMBOLIC LATTICE DOMAIN** )

Examiner: \*\*\*  
Art Unit: 2763

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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

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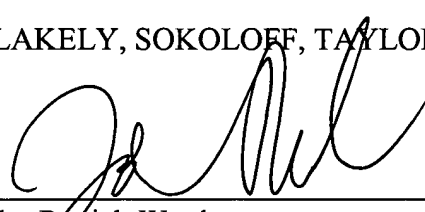
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Respectfully submitted,

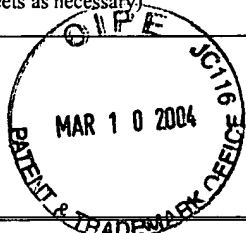
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Dated: 3/5/04

  
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|---|--|-------------------------------------|-----------------------------------|
| Substitute for Form 1449A/PTO (Modified)<br>(use as many sheets as necessary) |  | Attorney Docket No.:<br>42390.P9429 | Application Number:<br>09/608,637 |
| Sheet 1 of 1  |  | First Named Inventor:<br>Jin Yang   | Examiner:<br>Unassigned           |
|   |  | Filing Date:<br>June 30, 2000       | Art Unit:<br>2763                 |



**OTHER ART - NO PATENT LITERATURE DOCUMENTS**

| Examiner Initials* | Cite No <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published | Translation <sup>2</sup> |
|--------------------|----------------------|--|--------------------------|
|                    |                      | BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998  |                          |
|                    |                      | BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Volume 13, Issue 4, April 1994, pp. 401-424  |                          |
|                    |                      | CAMPOS, S.V.A., "Symbolic Model Checking in Practice," <u>XII Symposium on Integrated Circuits and Systems Design</u> , 1999 Natal, Brazil - IEEE, September 1999, pp. 98-101  |                          |
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